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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,518	09/23/2003	Yukihiro Noguchi	65933-042	2566

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EXAMINER	
AMADIZ, RODNEY	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,518	NOGUCHI ET AL.	
	Examiner	Art Unit	
	Rodney Amadiz	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-8 and 11-14* is/are rejected.

7)☐ Claim(s) *3-5,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 6-8 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jinno et al. (USPGPUB 2001/0040547) in view of Kabuto et al. (U.S. Patent 5,151,689)

As to **Claim 1**, Jinno et al. teaches a signal transmission circuit, including: a plurality of signal paths which respectively transmit signals outputted from a plurality of different circuit elements (Fig. 3, Reference Numbers 63, 64, 65, 66 and 67); and an output path formed by connecting the plurality of signal paths (Fig. 3, note that the output of switches 64 are connected to "To 4"), wherein each of the plurality of signal paths includes a buffer element and a switching element which receives an output from the buffer element (Fig. 3, Reference Numbers 66 and 67), the output path is formed by connecting output lines of the switching elements (Fig. 3, note output of switch 64 "TO 4"), and wherein any of the switching elements in the plurality of signal paths is turned on according to an operational mode, and then a target signal is selected and outputted to the output path (Pg. 3, ¶ 36). Jinno et al. however, does not teach a buffer element disposed in the output path. Examiner cites Kabuto et al. to teach a buffer element disposed in the output path (Fig. 1A, Reference Number 24). At the time the invention

was made, it would have been obvious to a person of ordinary skill in the art to incorporate a buffer element in the output path as taught by Kabuto et al. in the signal transmission circuit taught by Jinno et al. in order to optimize output conditions such as strengthening the signal.

As to **Claims 2 and 11**, the modified circuit of Jinno et al. and Kabuto et al. teach the buffer elements disposed in a dispersed manner so that the target signal might obtain a desired output characteristic by passing through both the buffer elements provided in the plurality of signal paths and the buffer element provided in the output path. (Jinno et al.—Fig. 3, Reference Number 66 and Kabuto et al.—Fig. 1A, Reference Number 24—furthermore, note that the buffer elements are dispersed in such a manner that the target signal will have a desired output characteristic).

As to **Claim 6**, most of the limitations have already been discussed with respect to the rejection of claim1, with the exception of the display apparatus, including: a plurality of pixel circuits; a circuit block which sequentially drives the plurality of pixel circuits; a plurality of signal paths that transmit signals outputted from circuit elements in the circuit block which respectively correspond to a final stage of the circuit block, when the pixel circuits are driven in a forward or reverse direction. Jinno et al. teaches a plurality of pixel circuits (Fig. 1, note Pixel circuit in Display Area 4); a circuit block which sequentially drives the plurality of pixel circuits (Figs. 1 and 3, Reference Numbers 61 and 62); a plurality of signal paths that transmit signals outputted from circuit elements in the circuit block (Fig. 3, Reference Numbers 63, 64, 65, 66 and 67), which respectively correspond to a final stage of the circuit block, when the pixel circuits are

driven in a forward or reverse direction (Pg. 2, ¶ 34 and Fig. 3—note that although only 2 shift registers are shown in Figure 3 it is well known that bidirectional shift registers comprise shift registers that extended on either side of the two shown and furthermore comprise a final stage shift register on both ends which comprise signal paths).

As to **Claim 7**, Jinno et al. teaches the circuit block being a circuit which drives a data signal line for writing data to the plurality of pixel circuits (Pg. 3, ¶ 36).

As to **Claim 8**, Jinno et al. teaches the circuit block being a shift register, and the plurality of signal paths transmit signals outputted from a final-stage of the shift register (Pg. 3, ¶ 36—note that that bidirectional shift registers comprise shift registers that extended on either side of the two shown in Figure 3 and furthermore comprise a final stage shift register on both ends which comprise signal paths).

As to **Claim 12**, Jinno et al. teaches wherein the buffer elements provided in the plurality of signal paths are adjusted so as to have a substantially uniform characteristic therebetween (Fig. 3, note both buffer elements 66 having the same characteristics as the neighboring buffer elements).

As to **Claim 13**, the modified circuit of Jinno et al. and Kabuto et al. teach a signal path up to a connector pin from the final-stage circuit in the circuit block (Fig. – note Reference Numbers 61 and 62 connected to Reference Number 7), wherein the buffer element disposed in the vicinity of the circuit element and the buffer element disposed in the vicinity of the connector pin are provided in the signal path (See Rejection of Claim 1 to note where the buffer elements are positioned), and wherein the plurality of buffer elements necessary for a signal to be transmitted to finally have a

desired output characteristic are disposed in a dispersed manner (Jinno et al.—Fig. 3, Reference Number 66 and Kabuto et al.—Fig. 1A, Reference Number 24—furthermore, note that the buffer elements are dispersed in such a manner that a desired output characteristic will be achieved).

As to **Claim 14**, the modified circuit of Jinno et al. and Kabuto et al. teach a signal transmission circuit, including a signal path up to a connector pin from a circuit element disposed at a final stage of a circuit block which sequentially drives a plurality of pixel circuits (Fig. –note Reference Numbers 61 and 62 connected to Reference Number 7—See also Fig. 1, note Pixel circuit in Display Area 4), wherein a buffer element disposed in the vicinity of the circuit element and a buffer element disposed in the vicinity of the connector pin are provided in the signal path (See Rejection of Claim 1 to note where the buffer elements are positioned), and wherein the plurality of buffer elements necessary for a signal to be transmitted to finally have a desired output characteristic are disposed in a dispersed manner (Jinno et al.—Fig. 3, Reference Number 66 and Kabuto et al.—Fig. 1A, Reference Number 24—furthermore, note that the buffer elements are dispersed in such a manner that a desired output characteristic will be achieved).

Allowable Subject Matter

3. Claims 3-5, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney Amadiz whose telephone number is (571) 272-7762. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

R.A.

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6/21/06
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PRIMARY EXAMINER